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Application No. 09/896,071

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| **United States Patent Application** | **20020053063** |
| **Kind Code** | **A1** |
| **Bhattacharya, Debashis ; et al.** | **May 2, 2002** |

Process for automated generation of design-specific complex functional blocks to improve quality of synthesized digital integrated circuits in CMOS

The ***above mentioned patent application closely matches*** with US Patent ***6,460,166*** (assigned to IBM) entitled, "System and method for restructuring of logic circuitry" with Inventors: **Reddy; Lakshmi Narasimha** (Valhalla, NY); **Rosser; Thomas Edward** (Austin, TX)

and ***also closely matches with*** US patent ***6,282,695*** (assigned to IBM) entitled, "System and method for restructuring of logic circuitry" with Inventors: **Reddy; Lakshmi Narasimha** (Valhalla, NY); **Rosser; Thomas Edward** (Austin, TX)

Claims 10 and 11 of above mentioned patent application mention of a weakness which is exactly same as FIG 3 (Critical Path). The Drawings of the above mentioned patent application and US Patent ***6,460,166*** have a very close match as well. Even the titles are same (Compare "improve quality of synthesized digital integrated circuits" of above mentioned patent application and US patent ***6,460,166*** "restructuring of logic circuitry". US patent ***6,460,166*** restructures with AO (AND-OR) or OA (OR-AND) generalized (any number of inputs) to represent any ***design-specific cell*** or transistor level circuit versus above mentioned patent application using transistor-level representation. Any logic function can be represented as AND-OR or OR-AND as any one skilled in this art may attest for CMOS.

Besides transistor level software has been around for the last 15 years in commercial practice at IBM and various Universities (particularly) University of California at Berkeley has several public domain program called MIS, MISII, SIS used throughout the universities and industry. Several articles in IEEE including IEEE transactions on CAD provide extensive details (as far back as 1987) of Professor DeMicheli's work at Stanford University and at IBM with various transistor level software synthesis for CMOS.

Anyway, this generalized transistor level software patent application should ***not be allowed*** as all known transistor level styles (domino, complex gate) have been presented and used for a long time.